

## Patent Claims

1. An evaluation circuit for detecting and/or  
5 locating faulty data words in a data stream  $T_n$   
comprising the following features:

- a first linear automaton circuit (L1) and also a  
second linear automaton circuit (L2) connected in  
parallel, each having a set of states  $z(t)$ ,
- 10 - the first linear automaton circuit (L1) and the  
second linear automaton circuit (L2) have a common  
input line for receiving a data stream  $T_n$   
comprising  $n$  successive data words  $y(1), \dots, y(n)$   
each having a width of  $k$  bits,
- 15 - the first linear automaton circuit (L1) can be  
described by the following equation

$$z(t+1) = Az(t) \oplus y(t)$$

- 20 - the second linear automaton circuit (L2) can be  
described by the following equation

$$z(t+1) = Bz(t) \oplus y(t)$$

25 where  $A$  and  $B$  represent the state matrices of the  
linear automaton circuits (L1, L2), where the  
state matrices  $A$  and  $B$  can be inverted, and where  
the dimension  $L$  of the state vectors is  $\geq k$ ,

- the first linear automaton circuit (L1) and the  
30 second linear automaton circuit (L2) are designed  
such that a first signature (S1) and a second  
signature (S2), respectively, can be calculated,
- $L$  first logic combination gates ( $XOR_{L1}$ ) arranged  
downstream of the first linear automaton circuit  
35 (L1) and also  $L$  second logic combination gates  
( $XOR_{L2}$ ) arranged downstream of the second linear  
automaton circuit (L2),

- the logic combination gates ( $XOR_{L1}$ ,  $XOR_{L2}$ ) are designed such that the signature ( $S1$ ,  $S2$ ) respectively calculated by the linear automaton circuit ( $L1$ ,  $L2$ ) can be compared with a  
5 predetermined good signature and a comparison value can be output.

2. The evaluation circuit as claimed in claim 1, characterized in that  
10 the logic combination gates ( $XOR_{L1}$ ,  $XOR_{L2}$ ) are present as exclusive-OR gates whose first inputs are respectively connected to the outputs of the associated linear automaton circuit ( $L1$ ,  $L2$ ) and to whose second inputs good signatures can be applied.

15 3. The evaluation circuit as claimed in claim 1 or 2, characterized in that arranged upstream of the first linear automaton circuit ( $L1$ ) is a first coder ( $C1$ ), which codes the data word  
20  $y(i)$  having the data word length of  $k$  bits into a coded data word  $u^1(i)$ ,  $u^1(i) = \text{Cod1}(y(i))$  having the word width of  $K1$  bits, for  $i=1, \dots, n$ , and where  $\text{Cod1}$  represents the coding function of the first coder ( $C1$ ).

25 4. The evaluation circuit as claimed in claim 3, characterized in that the following holds true for the coding function of the first coder ( $C1$ ):

30 
$$\text{Cod1}(y'(i)) = u^1(i) \oplus f_1(e(i)),$$

or

$$\text{Cod1}(y'(i)) = \text{Cod1}(y(i) \oplus e(i)) = \text{Cod1}(y(i) \oplus f_1(e(i)))$$

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where a function  $f_1$  by  $f_1(0) = 0$  exists for  $y'(i) = y(i) \oplus e(i)$ , and where a function  $f_1^{-1}$  where

$$f_1^{-1}(f_1(e)) = e$$

exists for all binary data words  $e$  having the word width  $k$  which may occur as errors of a data word, where  
 5  $e$  denotes a faulty data word of the data stream  $T_n$ .

5. The evaluation circuit as claimed in one of claims 1 to 4, characterized in that  
 10 arranged upstream of the second linear automaton circuit (L2) is a second coder (C2), which codes the data word  $y(i)$  having the data word length of  $k$  bits into a coded data word  $u^2(i)$ ,  $u^2(i) = \text{Cod2}(y(i))$  having the word width of  $K_2$  bits, for  $i=1, \dots, n$ , and where  
 15  $\text{Cod2}$  represents the coding function of the second coder (C2).

6. The evaluation circuit as claimed in claim 5, characterized in that  
 20 the following holds true for the coding function of the second coder (C2):

$$\text{Cod2}(y'(i)) = u^2(i) \oplus f_2(e(i)),$$

25 or

$$\begin{aligned} \text{Cod2}(y'(i)) &= \text{Cod2}(y(i) \oplus e(i)) \\ &= \text{Cod2}(y(i)) \oplus f_2(e(i)) \end{aligned}$$

30 where a function  $f_2^{-1}$  where

$$f_2^{-1}(f_2(e)) = e$$

exists for all binary data words  $e$  having the word  
 35 width  $k$  which may occur as errors of a data word, where  $e$  denotes a faulty data word of the data stream  $T_n$ .

7. The evaluation circuit as claimed in one of claims 3 to 6, characterized in that the word width  $K1$  of the data words  $u^1(i)$  coded by the first coder (C1) is equal to the word width  $K2$  of the data words  $u^2(i)$  coded by the second coder (C2).

8. The evaluation circuit as claimed in one of claims 3 to 7, characterized in that the first coder (C1) matches the second coder (C2) with regard to its construction and its function.

9. The evaluation circuit as claimed in one of claims 3 to 8, characterized in that the word width  $K1$  of the data words  $u^1(i)$  coded by the first coder (C1) and the word width  $K2$  of the data words  $u^2(i)$  coded by the second coder (C2) are in each case equal to the word width  $k$  of the data words  $y(1), \dots, y(n)$  of the data stream  $T_n$ .

10. The evaluation circuit as claimed in one of claims 3 to 9, characterized in that the coding functions  $Cod1$  and  $Cod2$  of the first coder and of the second coder (C2) are designed as follows:

$$\begin{aligned} & Cod1(y_1(i), y_2(i), \dots, y_k(i)) \\ & = P1(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0) \end{aligned}$$

$$\begin{aligned} & Cod2(y_1(i), y_2(i), \dots, y_k(i)) \\ & = P2(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0) \end{aligned}$$

for  $i, 1, \dots, n$

where the number of zeros situated at the end of  $P1(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0)$  is equal to

(K1-k), where the number at the end of  $P2(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0)$  is equal to (K2-k), and where P1 represents an arbitrary permutation of the K1 components of  $(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0)$  and  
 5 P2 represents an arbitrary permutation of the K2 components of  $(y_1(i), y_2(i), \dots, y_k(i), 0, \dots, 0)$ .

11. The evaluation circuit as claimed in one of claims 3 to 9,  
 10 characterized in that the coding functions Cod1 and Cod2 of the first coder and of the second coder (C2) are designed as follows:

$$\begin{aligned} & \text{Cod1}(y_1(i), y_2(i), \dots, y_k(i)) \\ 15 \quad & = P1(y_1(i), y_2(i), \dots, y_k(i), b_1^1, \dots, b_{K1-k}^1) \end{aligned}$$

$$\begin{aligned} & \text{Cod2}(y_1(i), y_2(i), \dots, y_k(i)) \\ & = P2(y_1(i), y_2(i), \dots, y_k(i), b_1^2, \dots, b_{K2-k}^2) \end{aligned}$$

20 where  $b_1^1, \dots, b_{K1-k}^1, b_1^2, \dots, b_{K2-k}^2 \in \{0,1\}$ , and where P1 and P2 represent arbitrary permutations.

12. The evaluation circuit as claimed in one of claims 3 to 11,  
 25 characterized in that the coding function Cod1 of the first coder (C1) is designed such that it realizes a linear block code,  $f_1 = \text{Cod1}$ .

30 13. The evaluation circuit as claimed in one of claims 3 to 9 or as claimed in claim 12, characterized in that the coding function Cod2 of the second coder (C2) is designed such that it realizes a linear block code,  
 35  $f_2 = \text{Cod2}$ .

14. The evaluation circuit as claimed in one of claims 1 to 13,

characterized in that  
the state matrix A of the first linear automaton  
circuit (L1) and the state matrix B of the second  
linear automaton circuit (L2) are related to one  
5 another as follows:

$$B = A^n$$

where  $n \neq 1$ .

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15. The evaluation circuit as claimed in one of  
claims 1 to 14,

characterized in that

the state matrix B of the second linear automaton  
15 circuit (L2) is equal to the inverted state matrix  $A^{-1}$   
of the first linear automaton circuit (L1).

16. The evaluation circuit as claimed in one of  
claims 1 to 15,

20 characterized in that

the first linear automaton circuit (L1) is designed as  
a linear feedback shift register and the second linear  
automaton circuit (L2) is designed as an inverse linear  
feedback shift register, both linear automaton circuits

25 (L1, L2) having a parallel input.

17. The evaluation circuit as claimed in one of  
claims 1 to 16,

characterized in that

30 the first linear automaton circuit (L1) is designed as  
a linear feedback, K1-dimensional multi-input shift  
register and/or the second linear automaton circuit  
(L2) is designed as a linear feedback, K2-dimensional  
multi-input shift register.

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18. The evaluation circuit as claimed in claim 17,  
characterized in that

the multi-input shift register/registers (L1, L2) has/have a primitive feedback polynomial of maximum length.

5 19. A method for detecting and/or locating faulty data words in a data stream  $T_n$ , the method having the following method steps of:

- a) inputting data words  $y(1), \dots, y(i-1), y'(i), y(i+1), \dots, y(n)$  of a data stream  $T_n$  into a first  
10 coder (C1),
- b) coding the data words  $y(1), \dots, y(n)$  into coded data words  $u^1(1), \dots, u^1(n)$  having the word width  $K_1$  where  $K_1 \geq k$  by means of the coding function  $Cod_1$  of the first coder (C1),
- 15 c) inputting the coded data words  $u^1(1), \dots, u^1(i-1), u^{1'}(i)$  or  $u^1(i), u^1(i), \dots, u^1(n)$  into the inputs of a first linear automaton circuit (L1), which is described by the automaton equation

20 
$$z^1(t+1) = A \cdot z^1(t) + u^1(t)$$

where  $z^1$  represents a  $K_1$ -dimensional state vector and  $A$  represents a  $K_1 \times K_1$  state matrix, and where the state matrix  $A$  can be inverted,

- 25 d) processing the coded data words  $u^1(1), \dots, u^1(i-1), u^{1'}(i)$  or  $u^1(i), u^1(i), \dots, u^1(n)$  by means of the first linear automaton circuit (L1), the first linear automaton circuit (L1)
  - undergoing transition to the state  
30  $z^1(n+1) = S_1(L1, y(1), \dots, y(i-1), y(i), y(i+1), \dots, y(n))$  if no error can be detected in the case of the coded data words  $u^1(1), \dots, u^1(i-1), u^1(i), u^1(i+1), \dots, u^1(n)$ ,
  - undergoing transition to the state  
35  $z^{1'}(n+1) = S_1(L1, y(1), \dots, y(i-1), y'(i), y(i+1), \dots, y(n))$  if an error is present at least in the case of the  $i$ -th position of the

coded data words  $u^1(1), \dots, u^1(i-1), u^{1'}(i), \dots, u^1(n),$

the signature of an error-free data stream  $T_n$  being designated by  $S(L1, y(1), \dots, y(i-1), y(i), y(i+1), \dots, y(n))$  and the signature of a faulty data stream  $T_n$  being designated by  $S(L1, y(1), \dots, y(i-1), y'(i), y(i+1), \dots, y(n)),$

e) checking the determined signature of the data stream  $T_n$  and continuing with method step a) for further data streams  $T_n$  if the determined signature of the data stream  $T_n$  is the signature of an error-free data stream  $T_n,$

f) inputting the data words  $y(1), \dots, y(i-1), y'(i), \dots, y(n)$  of the data stream  $T_n$  in a second coder (C2),

g) coding the data words  $y(1), \dots, y(i-1), y'(i), y(i+1), \dots, y(n)$  to coded data words  $u^2(1), \dots, u^2(i-1), u^{2'}(i)$  or  $u^2(i), u^2(i), \dots, u^2(n)$  having the word width  $K2$  where  $K2 \geq k$  by means of the coding function  $Cod2$  of the second coder (C2),

h) inputting the coded data words  $u^2(1), \dots, u^2(i-1), u^{2'}(i)$  or  $u^2(i), u^2(i), \dots, u^2(n)$  into the inputs of a second linear automaton circuit (L2), which is described by the automaton equation

$$z^2(t+1) = B \cdot z^2(t) \oplus u^2(t)$$

where  $z^2$  represents a  $K2$ -dimensional state vector and  $B$  represents a  $K2 \times K2$  state matrix where  $B \neq A$ , and where the state matrix  $B$  can be inverted,

i) processing the coded data words  $u^2(1), \dots, u^2(i-1), u^{2'}(i)$  or  $u^2(i), u^2(i), \dots, u^2(n)$  by means of the second linear automaton circuit (L2), the second linear automaton circuit (L2)

- undergoing transition to the state  $z^2(n+1) = S_2(L2, y(1), \dots, y(i-1), y(i), y(i+1), \dots, y(n))$  if no error can be detected in the

case of the data words  $u^2(1), \dots, u^2(i-1),$   
 $u^2(i), u^2(i), \dots, u^2(n),$   
- undergoing transition to the state  
 $z^{2'}(n+1)=S_2(L2, y(1), \dots, y(i-1), y(i), y'(i),$   
5  $y(i+1), \dots, y(n))$  if an error is present at  
least in the case of the  $i$ -th position of the  
coded data words  $u^2(1), \dots, u^2(i-1), u^{2'}(i),$   
 $u^2(i), \dots, u^2(n),$   
the signature of an error-free data stream  $T_n$   
10 being designated by  $S(L2, y(1), \dots, y(i-1), y(i),$   
 $y(i+1), \dots, y(n))$  and the signature of a faulty  
data stream  $T_n$  being designated by  $S(L2, y(1),$   
 $\dots, y(i-1), y'(i), \dots, y(n)),$   
j) determining the signature differences  $\Delta S1$  and  $\Delta S2$   
15 by means of exclusive-OR logic combinations of the  
signatures  $S1$  and  $S2$  determined in method step d)  
and i), respectively, with ascertained good  
signatures, in each case according to the  
following specifications:  
20  
 $\Delta S1= S(L1, y(1), \dots, y(i-1), y(i), y(i+1), \dots, y(n))$   
 $\oplus S(L1, y(1), \dots, y(i-1), y'(i), y(i+1) \dots, y(n))$   
 $\Delta S2= S(L2, y(1), \dots, y(i-1), y(i), y(i+1), \dots, y(n))$   
25  $\oplus S(L2, y(1), \dots, y(i-1), y'(i), y(i+1), \dots, y(n))$   
k) determining a unique solution for the position  $i$   
of the faulty bit in the faulty data word by  
solving the equation  
30  
 $f_1^{-1}(A^{i-n}\Delta S1)=f_2^{-1}(B^{i-n}\Delta S2)$   
and if no unique solution results for  $1 \leq i \leq n,$   
outputting a notification by means of an output  
35 medium that two or more errors are present in the  
data stream  $T_n$  under consideration,

- l) determining a unique solution for the counter  $e(i)$  of the faulty data word  $y'(i)$  in the data stream  $T_n$  by solving the equation

5 
$$e(i) = f_1^{-1}(A^{i-n} \cdot \Delta S1)$$

- m) outputting the position  $i$  of the faulty bit in the faulty data word and also the error  $e(i)$  of the faulty data word  $y'(i)$  in the data stream  $T_n$  by means of an output medium.
- 10

20. The method as claimed in claim 19, characterized in that the method steps are carried out by means of an evaluation circuit as claimed in one of claims 1 to 18.

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21. The evaluation circuit as claimed in one of claims 1 to 18, characterized in that the evaluation circuit is monolithically integrated on an integrated circuit.

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22. A loadboard for receiving at least one needle card for testing integrated circuits and/or having at least one test socket for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits, the loadboard having an evaluation circuit as claimed in one of claims 1 to 18.

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23. A needle card for testing integrated circuits, in which an evaluation circuit as claimed in one of claims 1 to 18 is integrated.

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24. A tester for testing integrated circuits having the following features:

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- the tester is provided with a plurality of instruments for generating signals or data streams

and with a plurality of measuring sensors, in particular for currents and voltages,

- the tester has a loadboard which is provided for receiving at least one needle card for testing integrated circuits and/or for connecting a handler to a tester of integrated circuits and/or which is equipped with at least one test socket for testing integrated circuits, and

- the tester has an evaluation circuit as claimed in one of claims 1 to 18.

25. A computer program for executing a method for detecting and/or locating faulty data words in a data stream  $T_n$ , which is designed such that at least the method steps a) and also k), l) and m) as claimed in claim 19 or 20 can be executed.

26. The computer program as claimed in claim 25, which is contained on a storage medium, in particular in a computer memory or in a random access memory.

27. The computer program as claimed in claim 25, which is transmitted on an electrical carrier signal.

28. A data carrier having a computer program as claimed in claim 25.

29. A method in which a computer program as claimed in claim 24 is downloaded from an electronic data network such as, by way of example, from the Internet onto a computer connected to the data network.